

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1 1. (Original) A multistage bit stream multiplexer having a switchable forward/reverse clock  
2 relationship comprising:  
3 a first multiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate  
4 and that produces a second plurality of bit streams at a second bit rate, wherein the first plurality of bit  
5 streams are greater in number than the second plurality of bit streams are in number, and wherein the first  
6 bit rate is less than the second bit rate;  
7 a second multiplexing integrated circuit that receives the second plurality of bit streams and that  
8 outputs at least one high-speed bit stream at a line bit rate that exceeds the second bit rate; and  
9 a clock circuit, wherein the clock circuit generates a forward transmit clock for use by the first  
10 multiplexing integrated circuit in producing the second plurality of bit streams based upon a reference  
11 clock signal selectable from a plurality of inputs, wherein the inputs include a reverse transmit clock  
12 generated by the second multiplexing integrated circuit.
- 1 2. (Original) The multistage bit stream multiplexer of claim 1, further comprising:  
2 a communication Application Specific Integrated Circuit (ASIC) from which the first  
3 multiplexing integrated circuit receives the first plurality of bit streams; and  
4 a media interface that receives the at least one high-speed bit stream and produces a media output.
- 1 3. (Original) The multistage bit stream multiplexer of claim 1, wherein the plurality of inputs further  
2 comprises an external oscillator output.
- 1 4. (Original) The multistage bit stream multiplexer of claim 1, wherein the plurality of inputs further  
2 comprises a voltage controlled oscillator output.
- 1 5. (Original) The multistage bit stream multiplexer of claim 1, wherein the reference clock signal is  
2 selected based upon a clock selector input.

- 1 6. (Original) The multistage bit stream multiplexer of claim 5, wherein the first multiplexing  
2 integrated circuit further comprises a phase locked loop (PLL) that receives the reference clock signal and  
3 produces a PLL Data Clock having a frequency equal to the second bit rate, and wherein a plurality of  
4 latches receive the PLL Data Clock, latch data multiplexed from the first plurality of bit streams and  
5 produce the second plurality of bit streams.
- 1 7. (Original) The multistage bit stream multiplexer of claim 6, wherein the frequency of the PLL  
2 Data Clock is 16 times the frequency of the reference clock
- 1 8. (Original) The multistage bit stream multiplexer of claim 7, further comprising a division circuit  
2 that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.
- 1 9. (Original) The multistage bit stream multiplexer of claim 1, wherein the forward transmit clock is  
2 a source centered double data rate clock with respect to each of the plurality of second bit streams.
- 1 10. (Currently Amended) The multistage bit stream multiplexer of claim 6, wherein the PLL outputs  
2 to the second multiplexing integrated circuit, a lock detect signal that remains active while the PLL is  
3 locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference  
4 clock signal, and wherein the first multiplexing integrated circuit selects the reverse clock through ~~the~~  
5 ~~clock selector~~ the clock selector input when the PLL is not locked to the reference clock signal.
- 1 11. (Original) The multistage bit stream multiplexer of claim 1, wherein the first multiplexing  
2 integrated circuit generates the reverse clock based on an external oscillator reference clock.
- 1 12. (Currently Amended) The multistage bit stream multiplexer of claim 4, wherein the first  
2 multiplexing integrated circuit further comprises a phase detector that receives a first input from a loop  
3 timing circuit and a second input from ~~one of the plurality of inputs~~ one of the plurality of inputs.
- 1 13. (Original) The multistage bit stream multiplexer of claim 1, wherein the first multiplexing  
2 integrated circuit comprises integrated circuits formed on a silicon substrate and the second multiplexing  
3 integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and  
4 Si.

1 14. (Currently Amended) An upstream multiplexing integrated circuit within a multi-stage bit stream  
2 multiplexer that operates with a switchable forward/reverse lock relationship with ~~an downstream a~~  
3 downstream multiplexing integrated circuit, comprising:

4 a plurality of input ports operable to receive a first plurality of bit streams at a first bit rate;  
5 a plurality of output ports to output a second plurality of bit streams at a second bit rate, wherein  
6 the first plurality of bit streams is greater in number than the second plurality of bit streams are in number,  
7 and wherein the first bit rate is less than the second bit rate; and

8 a clock ~~circuit, that generates~~ circuit that generates a forward transmit clock signal for use by the  
9 upstream multiplexing integrated circuit in producing the second plurality of bit streams based upon a  
10 reference clock signal selectable from a plurality of inputs, wherein said ~~inputs including~~ inputs include a  
11 reverse transmit clock generated by the downstream integrated circuit.

1 15. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the first plurality of  
2 bit streams are received from a communication Application Specific Integrated Circuit (ASIC) from  
3 which the first multiplexing integrated circuit receives the first plurality of bit streams, and wherein the  
4 downstream multiplexing integrated circuit outputs at least one high-speed bit stream to a media interface  
5 that produces a media output.

1 16. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the plurality of  
2 inputs further comprises an external oscillator output.

1 17. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the plurality of  
2 inputs further comprises a voltage-controlled oscillator.

1 18. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the reference clock  
2 signal is selected based upon a clock selector input.

1 19. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 13~~ claim 14, further  
2 comprising a phase locked loop (PLL) that receives the reference clock signal and produces a PLL Data  
3 Clock having a frequency equal to the second bit rate, wherein a plurality of latches receive the PLL Data  
4 Clock, latch data multiplexed from the first bit streams and produce the plurality of second bit streams.

1 20. (Original) The upstream multiplexing integrated circuit of claim 19, wherein the frequency of the  
2 PLL Data Clock comprises 16 times the frequency of the reference clock.

1 21. (Original) The upstream multiplexing integrated circuit of claim 19, further comprising a division  
2 circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit  
3 clock.

1 22. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the forward transmit  
2 clock is a source centered double data rate clock with respect to the second plurality of bit streams.

1 23. (Currently Amended) The upstream multiplexing integrated circuit of claim 19, wherein the PLL  
2 outputs to the upstream multiplexing integrated circuit, a lock detect signal that remains active while the  
3 PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the  
4 reference clock signal, and wherein the downstream multiplexing integrated circuit selects the reverse  
5 clock through ~~the clock selector~~ a clock selector input when the PLL is not locked to the reference clock.

1 24. (Original) The upstream multiplexing integrated circuit of claim 14, wherein the reverse clock is  
2 based on an external oscillator reference clock.

1 25. (Original) The upstream multiplexing integrated circuit of claim 19, further comprising a phase  
2 detector that receives a first input from a loop clock and a second input from the voltage controlled  
3 oscillator.

1 26. (Currently Amended) The upstream multiplexing integrated circuit of ~~claim 13~~ claim 14, further  
2 comprising a Si substrate, and wherein the downstream multiplexing integrated circuit comprises a  
3 substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second  
4 multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.

1 27. (Currently Amended) A method of multiplexing a first plurality of bit streams to at least one  
2 high-speed bit stream with a multistage multiplexer, comprising ~~the steps of~~:  
3 receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first  
4 bit rate;  
5 multiplexing the ~~first plurality of bit stream~~ first plurality of bit streams into a second plurality of  
6 bit streams at a second bit rate, wherein the second bit rate exceeds the first bit rate;  
7 receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a  
8 second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of  
9 bit streams is in number;  
10 multiplexing the ~~second plurality of bit stream~~ second plurality of bit streams into ~~at least one~~  
11 ~~high-speed bit streams~~ the at least one high-speed bit stream having a line bit rate that exceeds the second  
12 bit rate; and  
13 generating a forward transmit clock from a reference clock signal selectable from a plurality of  
14 inputs, wherein the plurality of inputs ~~comprise~~ include a reverse transmit clock generated by the second  
15 stage multiplexing integrated circuit.

1 28. (Currently Amended) The method of claim 27 wherein further comprising ~~the step of~~ producing a  
2 lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein a reverse  
3 transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.

1 29. (Currently Amended) The method of claim 27, wherein the first plurality of bit streams are  
2 received from a communication Application Specific Integrated Circuit (ASIC), and wherein the second  
3 stage multiplexing integrated circuit outputs ~~at least one high-speed bit stream~~ the at least one high speed  
4 bit stream to a media interface that produces a media output.

1 30. (Original) The method of claim 27, wherein the plurality of inputs comprises an external  
2 oscillator output.

1 31. (Original) The method of claim 27, wherein the plurality of inputs further comprises a voltage-  
2 controlled oscillator.

1 32. (Original) The method of claim 27, further comprising the step of selecting the reference clock  
2 signal with a clock selector.

1 33. (Currently Amended) The method of claim 27, further ~~comprising the step of~~ comprises receiving  
2 the reference clock signal and producing a PLL Data Clock having a frequency equal to the second bit  
3 rate with a PLL, wherein a plurality of latches receive the PLL Data Clock, latch multiplexed data from  
4 the first bit streams and produce the plurality of second bit streams.

1 34. (Original) The method of claim 33, wherein the frequency of PLL. Data Clock is 16 times the  
2 frequency of the reference clock signal.

1 35. (Original) The method of claim 33, further comprising a division circuit that receives the PLL  
2 Data Clock and generates an output used to produce the forward transmit clock.

1 36. (Original) The method of claim 33, wherein the forward transmit clock is a source centered  
2 double data rate clock with respect to the second plurality of bit streams.

1 37. (Currently Amended) The method of claim 33, further ~~comprising the steps of~~ comprises:  
2 generating a lock detect signal that remains active while the PLL is locked to the reference clock  
3 signal and becomes inactive when the PLL is not locked to the reference clock signal; and  
4 selecting the reverse clock as the reference clock signal through ~~the clock selector~~ a clock selector  
5 when the PLL is not locked to the reference clock signal.

1 38. (Original) The method of claim 27, wherein the reverse clock is based on an external oscillator  
2 reference clock.

1 39. (Currently Amended) The method of claim 33, further ~~comprising~~ comprises a phase detector that  
2 receives a first input from a loop clock and a second input from the voltage controlled oscillator.

1 40. (Currently Amended) The method of claim 33, further ~~comprising~~ comprises a Si substrate, and  
2 wherein the downstream multiplexing integrated circuit ~~comprises~~ includes a substrate selected from the  
3 group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit  
4 comprises integrated circuits formed on a Si substrate.

1 41. (Currently Amended) A method of multiplexing a first plurality of bit streams to at least one  
2 high-speed bit stream with a multistage multiplexer, ~~comprising the steps of~~ comprises:  
3 receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first  
4 bit rate;  
5 multiplexing ~~the first plurality of bit stream~~ the first plurality of bit streams into a second plurality  
6 of bit streams at a second bit rate;  
7 receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a  
8 second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of  
9 bit streams are in number, and wherein the first bit rate is less than the second bit rate;  
10 multiplexing ~~the second plurality of bit stream~~ the second plurality of bit streams into the at least  
11 one high-speed bit streams at a line bit rate that exceeds the second bit rate; and  
12 generating a forward transmit clock from a reference clock signal selectable from a plurality of  
13 inputs, wherein the plurality of inputs ~~comprise~~ include a reverse transmit clock generated by the second  
14 stage multiplexing integrated circuit.

1 42. (Currently Amended) The method of claim 25 wherein further ~~comprises~~ comprising the step of  
2 producing a lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein a  
3 reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference  
4 clock.